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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,905	06/14/2005	H Bernhard Pogge	FIS920020139US1	5819

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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BLDG. 300-482
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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,905	POGGE ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15, 17/15, 18/15, 19/15, 20/15, 21/20/15, 23/15, 24/23/15, 25/15 and 26/15* is/are rejected.

7)☒ Claim(s) *16, 19/16, 22, 27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Re claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19/15, there is confusingly ambiguous antecedent basis for the language, "the wafer."

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15, 17/15, 18/15, 20/15, 21/20/15, 23/15 and 24/23/15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Gaul (5682062) and Hsu (5627106).

At column 1, line 66 to column 3, line 3; column 4, lines 4-24; column 6, line 5-51; column 7, line 64 to column 9, line 42; and column 11, lines 43-52; Gaul discloses the following:

Re claim 15: A method for fabricating a three-dimensional integrated device including a plurality of vertically stacked and interconnected wafers, the method comprising the steps of: providing a first wafer 400 having a front surface and a back surface, the first wafer having devices "integrated circuits" formed in a region adjacent to the front surface thereof; forming a "via" in the first wafer extending from the front surface, the via being characterized by a lateral dimension at the front surface; removing material from the first wafer at the back surface thereof; forming an opening 430 in the back surface of the first wafer, thereby exposing the via, the opening having a lateral dimension; forming a layer of conducting material 444 in said opening; providing a second wafer 230 having a front surface and a back surface, the second wafer having devices "circuits" formed therein adjacent to the front surface thereof; forming a stud 237 a on the front surface of the second wafer; on the front surface of the second wafer, the studs projecting vertically therefrom; aligning the stud to the opening in the

back surface of the first wafer; and bonding the second wafer to the first wafer, so that the stud makes electrical contact with the via.

Re claim 17: A method according to claim 15, wherein said step of removing material causes the wafer to have a thickness of less than 20/μm "several 1000 Å" / "10-40 microns".

Re claim 18: A method according to claim 15, further comprising the step of attaching a handling plate 116 to the front surface of the first wafer using a layer of bonding material 115.

Re claim 20: A method according to claim 15, further comprising the steps of: forming an additional opening 430 in the back surface of the first wafer; forming an additional layer of conducting material 444 in said additional opening; forming an additional stud 237 b on the front surface of the second wafer; and aligning the additional stud to the additional opening in the back surface of the first wafer; and wherein said step of bonding the second wafer to the first wafer forms a connection between the additional stud and the additional layer of conducting material.

Re claim 21: A method according to claim 20, wherein the additional layer of conducting material is inherently electrically insulated from the via (via 235).

To further clarify the disclosure of the second wafer having devices "circuits" formed therein adjacent to the front surface thereof and forming a

stud 237 a on the front surface of the second wafer, it is noted that the disclosure, including the cited Fig. 3, of Gaul is not limited to an absolute frame of reference or otherwise limited to a particular orientation, and it is inherent that there is a frame of reference wherein the surface from which the stud projects is a front surface. Furthermore, the devices are formed adjacent to the front surface at least because they are formed nearby the front surface. In addition, Gaul discloses forming a stud on the front surface at least because Gaul discloses forming a stud in close proximity and in contact with the front surface.

Although Gaul does not appear to explicitly disclose, "the additional layer of conducting material for conducting heat between the second wafer and the first wafer," the language "for conducting heat between the second wafer and the first wafer" is a statement of intended use of the material that does not appear to result in a structural difference between the claimed material and the material of Gaul. Further, because the material of Gaul appears to have the same structure as the claimed material, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed material from the material of Gaul. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI

1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Gaul does not appear to explicitly disclose the following:

Re claim 15: the opening having a lateral dimension greater than said lateral dimension of the via.

Nonetheless, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied prior art, the dimensions are for a

particular **unobvious** purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, Gaul does not appear to explicitly disclose the following:

Re claim 15: forming a layer of bonding material on the front surface of the second wafer, the studs projecting vertically therefrom; bonding the second wafer to the first wafer using the layer of bonding material.

Re claim 23: A method according to claim 15, wherein said bonding material is a thermoplastic material.

Re claim 24: A method according to claim 23/15, wherein the thermoplastic material is polyimide.

Nevertheless, at column 3, line 14 to column 4, line 2, Hsu discloses forming a layer of bonding material 30 on the front surface of a second wafer 25, studs 20 projecting vertically therefrom; bonding the second wafer

to a first wafer 40 using the layer of bonding material; wherein said bonding material is a thermoplastic material; wherein the thermoplastic material is polyimide. In addition, it would have been obvious to combine this disclosure of Hsu with the disclosure of Gaul because it would facilitate the bonding of Gaul.

Claims 25/15 and 26/15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul and Hsu as applied to claim 15, and further in combination with McFarland (20020074637).

Gaul does not appear to explicitly disclose the following:

Re claim 25: A method according to claim 15, further comprising the step of attaching the three-dimensional integrated device to a multichip module "multi-chip modules."

Re claim 26: A method according to claim 15, further comprising the step of attaching the three-dimensional integrated device to an insulating layer 434 having wiring 152 formed therein using a stud-via connection.

Nonetheless, at paragraphs 17 and 18, McFarland discloses attaching a three-dimensional integrated device 120, 130 to a multichip module; and attaching the three-dimensional integrated device to an insulating layer 110 having wiring 116 formed therein using a stud-via 150, 160 connection.

Furthermore, it would have been obvious to combine this disclosure of McFarland with the disclosure of Gaul and Hsu because it would facilitate external electrical connection.

To further clarify, McFarland discloses attaching a three-dimensional integrated device 120, 130 to a multichip module because McFarland discloses, "the stacked flip chip assembly 100 shown in FIG. 1 is not limited to connecting through flip chip attachment to only three dies 120, 130, and 140, any number of dies can be stacked and connected using such stacked flip chip arrangement."

In the alternative, claims 15, 17/15, 18/15, 20/15, 21/20/15, 23/15 and 24/23/15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul and Hsu as applied to claims 15, 17/15, 18/15, 20/15, 21/20/15, 23/15 and 24/23/15 supra, and further in combination with Glenn (6577013).

Gaul and Hsu does not appear to explicitly disclose the following:

Re claim 15: the opening having a lateral dimension greater than said lateral dimension of the via.

Regardless, at column 4, line 65 to column 5, line 5, Glenn discloses an opening having a lateral dimension greater than a lateral dimension of the via "the vias 32 can be made wider or narrower at one end than at the other." Moreover, it would have been obvious to combine this disclosure of

Glenn with the disclosure of the applied prior art because it would serve as a centering guide for the stud of the applied prior art.

Claims 16, 19/16, 22, 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 19/15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
18-Aug-07